REMARKS

In the Office Action, the Examiner provisionally rejected claims 1-2 and 12 on the ground of nonstatutory double patenting over claim 1 and 25 of the copending Application No. 10/062,992. The Examiner also rejected claim 1 under 35 U.S.C. §103(a) as being anticipated by the United States Patent 6,134,705 issued to Pedersen et al. ("Pedersen") in view of the United States Patent 6,925,088 to Moreaux ("Moreaux"). The Examiner also rejected claims 2-11 under §103(a) as being anticipated by Pedersen in view of Moreaux. The Examiner also rejected claims 12-25 under 35 U.S.C. §103(a) as being anticipated by United States Patent 6,134,705 issued to Pedersen et al. ("Pedersen") in view of the United States Patent 6,925,088 to Moreaux ("Moreaux"). Claims 1-25 remain pending in this application.

In this Amendment, Applicants have amended claims 1-2 and 12. Applicants have added or canceled any claims. Accordingly, claims 1-25 will be pending after entry of this Amendment.

I. Double Patenting Rejection

In the Office Action, the Examiner provisionally rejected claims 1-2 and 12 on the ground of nonstatutory double patenting over claim 1 and 25 of the copending Application No. 10/062,992. Applicants respectfully request that the double patenting rejection be placed on hold until the status of the claims in the current application and the copending application are finalized.

II. Rejection of Claim 1 under §103(a)

In the Office Action, the Examiner rejected claim 1 under §103(a) as being anticipated by Pedersen in view of Moreaux. Claim 1 recites a data storage structure that stores several combinational-logic sub-networks. Each sub-network performs a set of output functions and includes a set of circuit elements. At least some of the sub-networks include a first circuit that has a first output outside the sub-network and a second circuit that has a second output outside

the sub-network. The first circuit receives a direct or indirect input from the second circuit. Each sub-network is stored based on a set of indices derived from the set of output functions performed by the sub-network. The set of indices is used to retrieve the sub-network from the data storage structure.

Applicants respectfully submit that neither Pedersen nor Moreaux alone or in combination does disclose, teach, or even suggest such a data storage structure for at least the following reasons. *First*, in the Office Action, the Examiner has agreed that Pedersen does not specify sub-networks that include a first circuit that has a first output outside the sub-network and a second circuit that has a second output outside the sub-network, where the first circuit receives a direct or indirect input from the second circuit. *See,* Office Action, page 4. Applicants respectfully submit that Moreaux also does not disclose such sub-networks.

Specifically, in the Office Action, the Examiner has cited characters 301 and 302 in Figure 3 of Moreaux as a first circuit that has a first output outside the sub-network and a second circuit that has a second output outside the sub-network. Applicants respectfully submit that the cited Figure 3 of Moreaux does not show any of the entities labeled 301 and 302 to have outputs outside the shown structure. For instance, the entities labeled 301 are only connected to entities labeled 301, 302, and 303 that are inside the shown structure. Therefore, neither Moreaux nor Pedersen shows a first circuit that has a first output outside the sub-network and a second circuit that has a second output outside the sub-network.

Second, Applicants respectfully submit that Pedersen, Moreaux, or their combination does not disclose, teach, or even suggest a data storage structure that stores each sub-network based on a set of indices derived from the set of output functions performed by the sub-network. In the Office Action, the Examiner cited Figures 7E-7F; column 1, lines 37-44; column 11, lines 40-60; column 12, lines 10-15 and lines 43-45; and column 16, lines 21-39 of Pedersen for

specifying such a limitation. Applicants respectfully submit that neither in any of the cited figures and paragraphs, not in anywhere else Pedersen and/or Moreaux specify such a data storage structure.

Specifically, Figure 7E-7F and column 16, lines 21-39 of Pedersen specify how some hard registers and soft registers can be distinguished. Column 1, lines 37-44 is a part of the cross reference section citing a graphics editor and the Examiner has not specified what in this paragraph is related to limitations of claim 1. The other paragraphs cited by the Examiner specify the following:

> The sub-netlist contains the logic nodes that are affected by the design changes identified at step 353 (both directly and indirectly modified nodes). The compiler performs step 355 via a method which is the subject of this invention. Next, the compiler synthesizes the changed portion of the changed design at a step 357. To save resources, it typically does not synthesize the unchanged portion of the design.
> Now the newly synthesized sub-netlist may replace a corresponding portion of the original synthesized netlist. The original and changed synthesized netlists may optionally be compared against one another by netlist differencing. See step 359. This optional step confirms which nodes of the synthesized netlist have actually changed. Only those gates need be considered in subsequent incremental compilation procedures. The process is now complete at 365 and process control is directed to step 320 of process 300 (FIG. 3A). That is, the compiler now maps, partitions, and fits the changed gates of the synthesized netlist into logic cells while preserving as much of the original fitting as possible.

See, Pedersen, column 11, lines 40-60

> In overview, process 355 involves first identifying "external nodes" which are input/output pins and certain registers (defined below) common to both the synthesized original design and the unsynthesized changed design. Then, the compiler recurses forward from the new nodes to external nodes and, thereafter, recurses backward from those external nodes to the next external nodes in the path.

See, Pedersen, column 12, lines 10-15

> After the modified external gate or gates have been identified by forward recursion from the current new gate under consideration, the compiler must determine whether there are any new gates remaining to be considered.

See, Pedersen, column 12, lines 43-45

Applicants respectfully submit that, as it is clearly obvious from the above paragraphs, none of the figures and paragraphs cited by the Examiner disclose, teach, or even suggest a data storage structure that stores each sub-network based on a set of indices derived from the set of output functions performed by the sub-network.

Third, Moreaux is in the field of aircraft data transmission systems and the cited entities are star distributors (entities labeled 301) and peripheral devices (entities 302) (*See*, Moreaux, column 1, line 13, and column 3, lines 23-27), whereas Pedersen is in the field of incremental compilation of changed electronic designs, delineating the range of influence of a design change in an unsynthesized netlist (*See*, Pedersen, column 2, lines 25-29). Applicants respectfully submit that the Examiner's rejection has relied on impermissible piecemeal and hindsight combination of features from different references. Therefore, the Examiner has not identified any suggestions or motivations in the art for establishing this combination to arrive to a data storage structure for storing combinational-logic sub-networks. Applicants have amended claim 1 to clarify that the data storage structure is stores combinational-logic sub-networks. The Amendment is made for reasons of clarity and not for reasons of patentability. Applicants do not surrender any equivalents of the amended elements.

In view of the foregoing remarks, Applicants respectfully submit that the cited references, neither alone nor through their piecemeal, hindsight combination, render claim 1 invalid. Accordingly, Applicants respectfully request reconsideration and withdrawal of the 103(a) rejection of claim 1.

III. Rejection of Claims 2-11 under §103(a)

In the Office Action, the Examiner rejected claims 2-11 under §103(a) as being anticipated by Pedersen in view of Moreaux. Claims 3-11 are directly or indirectly dependent on

claim 11. Claim 2 recites a data storage structure that stores several combinational-logic sub-networks. Each sub-network performs a set of output functions and includes a set of circuit elements. At least some of the sub-networks include a first circuit that has a first output outside the sub-network and a second circuit that has a second output outside the sub-network. The first circuit receives a direct or indirect input from the second circuit. The data storage structure stores each sub-network based on a parameter derived from the set of output functions of the sub-network. The parameter is used to retrieve the sub-network from the data storage structure.

Applicants respectfully submit that neither Pedersen nor Moreaux alone or in combination does disclose, teach, or even suggest such a data storage structure for at least the following reasons. *First*, in the Office Action, the Examiner has agreed that Pederson does not specify sub-networks that include a first circuit that has a first output outside the sub-network and a second circuit that has a second output outside the sub-network, where the first circuit receives a direct or indirect input from the second circuit. *See,* Office Action, page 5. Applicants respectfully submit that Moreaux also does not disclose such sub-networks.

Specifically, in the Office Action, the Examiner has cited characters 301 and 302 in Figure 3 of Moreaux as a first circuit that has a first output outside the sub-network and a second circuit that has a second output outside the sub-network. Applicants respectfully submit that the cited Figure 3 of Moreaux does not show any of the entities labeled 301 and 302 to have outputs outside the shown structure. For instance, the entities labeled 301 are only connected to entities labeled 301, 302, and 303 that are inside the shown structure. Therefore, neither Moreaux nor Pedersen shows a first circuit that has a first output outside the sub-network and a second circuit that has a second output outside the sub-network.

Second, Applicants respectfully submit that Pedersen, Moreaux, or their combination does not disclose, teach, or even suggest a data storage structure that stores each sub-network

based on a parameter that is derived from the set of output functions of the sub-network. In the Office Action, the Examiner cited Figures 7E-7F; column 1, lines 37-44; column 11, lines 40-60; column 12, lines 10-15 and lines 43-45; and column 16, lines 21-39 of Pedersen for specifying such a limitation. Applicants respectfully submit that neither in any of the cited figures and paragraphs, not in anywhere else Pedersen and/or Moreaux specify such a data storage structure.

Specifically, Figure 7E-7F and column 16, lines 21-39 of Pedersen specify how some hard registers and soft registers can be distinguished. Column 1, lines 37-44 is a part of the cross reference section citing a graphics editor and the Examiner has not specified what in this paragraph is related to limitations of claim 2. The other paragraphs cited by the Examiner specify the following:

> The sub-netlist contains the logic nodes that are affected by the design changes identified at step 353 (both directly and indirectly modified nodes). The compiler performs step 355 via a method which is the subject of this invention. Next, the compiler synthesizes the changed portion of the changed design at a step 357. To save resources, it typically does not synthesize the unchanged portion of the design.
> Now the newly synthesized sub-netlist may replace a corresponding portion of the original synthesized netlist. The original and changed synthesized netlists may optionally be compared against one another by netlist differencing. See step 359. This optional step confirms which nodes of the synthesized netlist have actually changed. Only those gates need be considered in subsequent incremental compilation procedures. The process is now complete at 365 and process control is directed to step 320 of process 300 (FIG. 3A). That is, the compiler now maps, partitions, and fits the changed gates of the synthesized netlist into logic cells while preserving as much of the original fitting as possible.

See, Pedersen, column 11, lines 40-60

> In overview, process 355 involves first identifying "external nodes" which are input/output pins and certain registers (defined below) common to both the synthesized original design and the unsynthesized changed design. Then, the compiler recurses forward from the new nodes to external nodes and, thereafter, recurses backward from those external nodes to the next external nodes in the path.

See, Pedersen, column 12, lines 10-15

> After the modified external gate or gates have been identified by forward recursion from the current new gate under consideration, the compiler must determine whether there are any new gates remaining to be considered.

See, Pedersen, column 12, lines 43-45

Applicants respectfully submit that, as it is clearly obvious from the above paragraphs, none of the figures and paragraphs cited by the Examiner disclose, teach, or even suggest a data storage structure that stores each sub-network based on a set of indices derived from the set of output functions performed by the sub-network.

Third, Moreaux is in the field of aircraft data transmission systems and the cited entities are star distributors (entities labeled 301) and peripheral devices (entities 302) (*See*, Moreaux, column 1, line 13, and column 3, lines 23-27), whereas Pedersen is in the field of incremental compilation of changed electronic designs, delineating the range of influence of a design change in an unsynthesized netlist (*See*, Pedersen, column 2, lines 25-29). Applicants respectfully submit that the Examiner's rejection has relied on impermissible piecemeal and hindsight combination of features from different references. Therefore, the Examiner has not identified any suggestions or motivations in the art for establishing this combination to arrive to a data storage structure for storing combinational-logic sub-networks. Applicants have amended claim 2 to clarify that the data storage structure is stores combinational-logic sub-networks. The Amendment is made for reasons of clarity and not for reasons of patentability. Applicants do not surrender any equivalents of the amended elements.

In view of the foregoing remarks, Applicants respectfully submit that the cited references, neither alone nor through their piecemeal, hindsight combination, render claim 2 invalid. Given that claims 3-11 are dependent on claim 2, Applicants respectfully submit that these claims are allowable over the cited reference for at least the same reasons that were provided above for

claim 2. In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the 103(a) rejection of claims 2-11.

IV. Rejection of Claims 12-25 under §103(a)

In the Office Action, the Examiner rejected claims 12-25 under §103(a) as being anticipated by Pedersen in view of Moreaux. Claims 13-25 are directly or indirectly dependent on claim 11. Claim 12 recites a sub-network record management system that includes a data storage structure that stores a plurality of combinational-logic sub-networks. Each sub-network performs a set of output functions and includes a set of circuit elements. At least some of the sub-networks include a first circuit that has a first output outside the sub-network and a second circuit that has a second output outside the sub-network. The first circuit receives a direct or indirect input from the second circuit. The data storage structure stores each sub-network based on a parameter derived from the set of output functions of the sub-network. The parameter is used to retrieve the sub-network from the data storage structure. The sub-network record management system also includes a data access manager that identifies and retrieves sub-networks from the data storage structure.

Applicants respectfully submit that neither Pedersen nor Moreaux alone or in combination does disclose, teach, or even suggest such a sub-network record management system for at least the following reasons. *First*, Applicants respectfully submit that Pedersen, Moreaux, or their combination does not disclose, teach, or even suggest a sub-network record management system that has a data access manager that identifies and retrieves sub-networks from a data storage structure. Specifically, in the Office Action, the Examiner cited column 10, lines 40-50 and item 314 in Figure 3A of Pedersen for specifying such a system. Applicants respectfully submit that Figure 3A of Pedersen is a process flow diagram depicting how the incremental recompile methodologies of the invention may be incorporated into a standard

compilation/recompilation design flow. *See*, Pedersen, column 5, lines 23-27. Furthermore, item 314 in Figure 3A of Pedersen specifies: "Receive An Unsynchronized Netlist Of The Changed Design". Applicants respectfully submit that the entity that performs item 314 is process 300 which is the process showing how the incremental recompilation method of Pedersen can be incorporated into a standard compilation/recompilation design flow and is not a sub-network record management system that has a data access manager that identifies and retrieves sub-networks from a data storage structure.

Second, in the Office Action, the Examiner has agreed that Pedersen does not specify sub-networks that include a first circuit that has a first output outside the sub-network and a second circuit that has a second output outside the sub-network, where the first circuit receives a direct or indirect input from the second circuit. *See,* Office Action, page 9. Applicants respectfully submit that Moreaux also does not disclose such sub-networks.

Specifically, in the Office Action, the Examiner has cited characters 301 and 302 in Figure 3 of Moreaux as a first circuit that has a first output outside the sub-network and a second circuit that has a second output outside the sub-network. Applicants respectfully submit that the cited Figure 3 of Moreaux does not show any of the entities labeled 301 and 302 to have outputs outside the shown structure. For instance, the entities labeled 301 are only connected to entities labeled 301, 302, and 303 that are inside the shown structure. Therefore, neither Moreaux nor Pedersen shows a first circuit that has a first output outside the sub-network and a second circuit that has a second output outside the sub-network.

Third, Applicants respectfully submit that Pedersen, Moreaux, or their combination does not disclose, teach, or even suggest a sub-network record management system that includes a data storage structure that stores each sub-network based on a parameter that is derived from the set of output functions of the sub-network. In the Office Action, the Examiner cited Figures 7E-

7F; column 1, lines 37-44; column 11, lines 40-60; column 12, lines 10-15 and lines 43-45; and column 16, lines 21-39 of Pedersen for specifying such a limitation. Applicants respectfully submit that neither in any of the cited figures and paragraphs, not in anywhere else Pedersen and/or Moreaux specify such a data storage structure. Specifically, Figure 7E-7F and column 16, lines 21-39 of Pedersen specify how some hard registers and soft registers can be distinguished. Column 1, lines 37-44 is a part of the cross reference section citing a graphics editor and the Examiner has not specified what in this paragraph is related to limitations of claim 12. The other paragraphs cited by the Examiner specify the following:

> The sub-netlist contains the logic nodes that are affected by the design changes identified at step 353 (both directly and indirectly modified nodes). The compiler performs step 355 via a method which is the subject of this invention. Next, the compiler synthesizes the changed portion of the changed design at a step 357. To save resources, it typically does not synthesize the unchanged portion of the design.
> Now the newly synthesized sub-netlist may replace a corresponding portion of the original synthesized netlist. The original and changed synthesized netlists may optionally be compared against one another by netlist differencing. See step 359. This optional step confirms which nodes of the synthesized netlist have actually changed. Only those gates need be considered in subsequent incremental compilation procedures. The process is now complete at 365 and process control is directed to step 320 of process 300 (FIG. 3A). That is, the compiler now maps, partitions, and fits the changed gates of the synthesized netlist into logic cells while preserving as much of the original fitting as possible.

See, Pedersen, column 11, lines 40-60

> In overview, process 355 involves first identifying "external nodes" which are input/output pins and certain registers (defined below) common to both the synthesized original design and the unsynthesized changed design. Then, the compiler recurses forward from the new nodes to external nodes and, thereafter, recurses backward from those external nodes to the next external nodes in the path.

See, Pedersen, column 12, lines 10-15

> After the modified external gate or gates have been identified by forward recursion from the current new gate under consideration, the compiler must determine whether there are any new gates remaining to be considered.

See, Pedersen, column 12, lines 43-45

Applicants respectfully submit that, as it is clearly obvious from the above paragraphs, none of the figures and paragraphs cited by the Examiner disclose, teach, or even suggest a sub-network record management system that includes a data storage structure that stores each sub-network based on a set of indices derived from the set of output functions performed by the sub-network.

Fourth, Moreaux is in the field of aircraft data transmission systems and the cited entities are star distributors (entities labeled 301) and peripheral devices (entities 302) (*See*, Moreaux, column 1, line 13, and column 3, lines 23-27), whereas Pedersen is in the field of incremental compilation of changed electronic designs, delineating the range of influence of a design change in an unsynthesized netlist (*See*, Pedersen, column 2, lines 25-29). Applicants respectfully submit that the Examiner's rejection has relied on impermissible piecemeal and hindsight combination of features from different references. Therefore, the Examiner has not identified any suggestions or motivations in the art for establishing this combination to arrive to a data storage structure for storing combinational-logic sub-networks. Applicants have amended claim 12 to clarify that the data storage structure is stores combinational-logic sub-networks. The Amendment is made for reasons of clarity and not for reasons of patentability. Applicants do not surrender any equivalents of the amended elements.

In view of the foregoing remarks, Applicants respectfully submit that the cited references, neither alone nor through their piecemeal, hindsight combination, render claim 12 invalid. Given that claims 13-25 are dependent on claim 12, Applicants respectfully submit that these claims are allowable over the cited reference for at least the same reasons that were provided above for claim 12. In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the 103(a) rejection of claims 12-25.

CONCLUSION

In view of the foregoing, it is submitted that all pending claims, namely claims 1-25, are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance is earnestly solicited at the earliest possible date.

Respectfully submitted,

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